ABSTRACT OF THE DISCLOSURE

The sheet resistance of a gate electrode 8A (a word line) of memory cell selection MISFET Q a DRAM and a sheet resistance of bit lines BL_1, BL_2 are, respectively, 2 Ω/□ or below. Interconnections of a peripheral circuit are formed during the step of forming the gate electrode 8A (the word line WL) or the bit lines BL_1, BL_2 by which the number of the steps of manufacturing the DRAM can be reduced.